of the claimed invention but fails to teach that the semiconductor region of the first conductor type (p-well 164) has an equal concentration of impurity as the semiconductor substrate 114. Togei was cited in the Office Action and it was asserted that Togei teaches a semiconductor region of a first conduction type (P-type portion 1a) surrounded by a buried semiconductor layer (N-type buried layer 2) and by a semiconductor region (N^+-type input-output region 5 and P^+-type region 8), wherein a concentration of an impurity in the semiconductor region of the first conduction type 1a is equal to a concentration of an impurity in the semiconductor substrate 1. It was therefore asserted that it would have been obvious to modify the AAPA with Togei in order to derive the present invention. Applicants traverse the rejection and submit that claims 1-7 recite subject matter that is not shown, taught or otherwise suggested by the combination of cited prior art.

Claim 1, upon which claims 2-7 depend, recites a semiconductor device that includes a lightly doped semiconductor substrate of a first conduction type, a buried semiconductor layer of a second conduction type, a semiconductor region of the second conduction type, and a semiconductor region of the first conduction type. The buried semiconductor layer is formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate. The semiconductor region of the second conduction type extends from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer and is connected to the buried semiconductor layer. The semiconductor region of the first conduction type is formed in the semiconductor substrate surrounded by the buried semiconductor layer and the

semiconductor region of the second conduction type. The semiconductor region of the first conduction type is isolated from the semiconductor substrate by the buried semiconductor layer and the semiconductor region of the second conduction type. A concentration of an impurity in the semiconductor region of the first conduction type is equal to a concentration of an impurity in the semiconductor substrate

As a result of the claim configuration, the semiconductor region of the first conduction type is surrounded by the buried semiconductor layer of the second conduction type and the semiconductor region of the second conduction type. Thusly, the semiconductor region of the first conduction type is isolated from the substrate by the buried semiconductor layer of the second conduction type and the semiconductor region of the second conduction type. Since the semiconductor region of the first conduction type is isolated from the substrate, an advantage is obtained that it is possible to apply a voltage to the semiconductor region of the first conduction type, which is lower than a ground voltage of the semiconductor substrate.

Togei is directed to a semiconductor memory device. Referring to Figure 3 of Togei, the P-type portion 1a of a first conduction type is not surrounded by the buried semiconductor layer (N-type buried layer 2) of a second conduction type and the semiconductor region (N^+-type input-output region 5, P^+-type region 8) of the second conductor type, as required by claim 1 of the present invention. The N-type buried layer 2 and the N^+-type input-output region 5 of Togei are disconnected from each other. The N-type buried layer 2 and P^+-type region 8 are also disconnected from each other.

Therefore, in Togei, the P-type portion 1a is not isolated from the silicon substrate 1, and is different from the p-well 164 of the AAPA.

In Togei, since the N-type buried layer 2 functions as a member of a capacitor. Therefore, the N-type buried layer 2 needs to separate from the N^+-type input-output region 5 and the P^+-type region 8. If the N-type buried layer 2 is connected to the N^+-type input-output region 5 or the P^+-type region 8, information can not stored in the N-type buried layer 5. Moreover, the P-type portion 1a of Togei does not correspond to the p-well 164 of the Applicants' admitted prior art in the instant application. That is, in Togei, as described above, the P-type portion 1a is not surrounded by the buried semiconductor layer (N-type buried layer 2) and the semiconductor region (N^+-type input-output region 5, P^+-type region 8). The N-type buried layer 2 and the N^+-type input-output region 5 are disconnected from each other. The N-type buried layer 2 and P^+-type region 8 are disconnected from each other, and the P-type portion 1a is not isolated from the silicon substrate 1. In contrast, the AAPA shows a p-well 164 surrounded by an n-well 138. The reason why the p-well 164 is surrounded by the n-well 138 is for isolating the p-well 164 from substrate 114 by n-well 138. Therefore, the P-type portion 1a of Togei cannot be said to correspond to the p-well 164 of the AAPA, and therefore, there would have been no motivation to combine the teachings of Togei with the AAPA Even if such motivation existed, such combination would fail to render the claimed invention for the reasons above, and such combination would not have a likelihood of being successful.

Moreover, as defined by the claimed invention, a concentration of the impurity in the semiconductor region of the first conduction type is equal to a concentration of the impurity in the semiconductor substrate. In the present invention, the semiconductor region of the first conduction type is not implanted with the impurity ion. Therefore, in the present invention, the semiconductor region of the first conduction type is not damaged by the impurity ion implantation. Consequently, in the present invention, a leak current from a capacitor of a memory cell through a junction between a source/drain diffused layer and the semiconductor region is small, and frequent rewriting operations for retaining a charge of the capacitor are not necessary, whereby the semiconductor device can have small electric consumption. Such a technique of the present invention is neither disclosed nor suggested in the AAPA or in Togei.

Thus, the combination of cited prior art fails to show or suggest each and every element, and it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have combine the teaching of the AAPA with Togei, since such combination would still fail to render each and every element of the claimed invention. Accordingly, Applicants request that the rejection be withdrawn and claims 1-7 be allowed.

In view of the above remarks, the Applicants respectfully submit that each of claims 1-7 recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicants therefore request that each of claims 1-7 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not considered to be timely filed, Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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Petition for Extension of Time

MARKED-UP COPY OF CLAIM AMENDMENTS

1. (Four times amended) A semiconductor device comprising:

a lightly doped semiconductor substrate of a first conduction type;

a buried semiconductor layer of a second conduction type formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate;

a semiconductor region of the second conduction type extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer, the semiconductor region of the second conduction type being connected to the buried semiconductor layer; and

a semiconductor region of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type, the semiconductor region of the first conduction type being isolated from the semiconductor substrate by the buried semiconductor layer and the semiconductor region of the second conduction type,

wherein a concentration of an impurity in the semiconductor region of the first conduction type is [equally] equal to a concentration of an impurity in the semiconductor substrate.